11.6 A Single-Chip CMOS Transceiver for UHF Mobile RFID Reader

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Radio-frequency identification (RFID) application is growing rapidly in many areas such as supply chain managements, anti-fraud systems, and object tracking systems [1]. The mobile RFID technology currently integrates the RFID technology with the mobile communication network and enables the use of mobile phones to access the information from the tag. The RFID systems operating at low frequencies (125kHz or 13.56MHz) are limited in their data rates and distances. Due to the great demand for higher data rates, longer reading distances, and smaller antenna sizes, much attention has been paid to the UHF frequency-band RFID systems, especially for mobile phone applications [2-4].

In the return link of an RFID operation, the receiver of the reader listens to the response of tag (transponder) while the transmitter sends a continuous wave to the tag for power transfer. The most critical part is how to achieve a better isolation between the transmitter and the receiver. Conventionally, an RFID reader module contains two antennas because the isolation from transmitter to receiver is much better in a two-antenna reader than in a single-antenna reader. However, it is not suitable for the mobile phone reader system, due to the physical dimension and the cost problem [1]. In a single-antenna reader system, the backscattered desired signal returning from the tag is mixed with the transmitter carrier. The amount of transmitter carrier leakage, which is typically above 0dBm at the receiver input, is determined by the antenna reflection coefficient and the isolation of the directional coupler. The transmitter carrier leakage leads to the saturation of receiver block and degradation of the sensitivity. Therefore, P_{1dB} of the receiver front-end should be high enough to avoid the receiver saturation caused by the large transmitter carrier leakage. This paper decribes a CMOS RF transceiver for UHF mobile RFID reader operating at 900MHz band. The transceiver is designed and fabricated in a 0.18μm CMOS process. The design focus is on the linearity rather than the noise figure.

Figure 11.6.1 shows the block diagram of the single-chip RFID reader which integrates an RF transceiver, data converters, a digital baseband modem, an MPU, memory, and host interfaces. The designed UHF mobile RFID reader supports ISO/IEC 18000-6 type B and EPC Class-1 Generation-2 UHF standard [2-3]. Figure 11.6.2 shows the receiver architecture of the RF transceiver. Among various receiver architectures, the direct-conversion receiver (DCR) is adopted for the backscattering communication solution. In the DCR architecture, the transmitter carrier leakage to the receiver input is directly down-converted to DC. It can be removed by the DC-offset cancellation feedback loop. The linearity of the conventional Gilbert-cell mixer is not satisfactory mainly because of the transconductance nonlinearity which becomes more serious especially at lower bias current. High linearity of the receiver front-end is achieved by using a CMOS passive switching mixer, as shown in Fig. 11.6.2. Its linearity is excellent since the passive FET switches are very linear due to the low impedance and no transconductance nonlinearity. To cope with very large transmitter carrier leakage, the LNA can be bypassed in the normal-mode operation and it is used optionally. The flicker noise of the CMOS mixer is a critical issue in DCRs. The passive switching mixer has very low 1/f noise because there is no DC current through the switching stage [5]. In the baseband analog parts, the local dc feedback loop is used for cancellation of the DC offset which is downconverted from the transmitter carrier leakage. Active-RC implementations of low-pass filters and opamp-based programmable-gain amplifiers (PGAs) are used for their excellent linearity performance. The gain of the PGA in decibels changes linearly with a resolution of 1dB and control range of 63dB by digitally controlled 6b switches.

The transmitter is also implemented using a direct I/Q upconversion architecture as shown in Fig. 11.6.3. The transmitter supports both single-side-band (SSB) and double-side-band (DSB) modulation for the reader-to-tag communication and it sends a unmodulated carrier for the tag-to-reader communication. In the upconversion mixer, I/Q baseband signals are upconverted to 900MHz band and added together. The source degeneration transconductance cells are used for linearity performance to satisfy the transmitter spectrum mask. An active load is used for the upconversion mixer output to reduce the chip area. The drive amplifier is a cascode type with an external RF choke load. The cascode configuration is used for better isolation between input and output stage. The maximum output power of the drive amplifier is 4dBm and the power can be controlled digitally by switching the transconductance of the parallel array of the input transistor with a control range of 13dB. The external power amplifier is used for maximum output power of 30dBm.

A fractional-N frequency synthesizer is designed for high-frequency resolution as shown in Fig. 11.6.4. The 900MHz differential I/Q LO signals are obtained by dividing differential signals from an integrated 1.8GHz LC-VCO. In the VCO, PMOS and NMOS cross-coupled pairs are used for symmetry with a differential on-chip inductor in the tank circuit. In order to reduce the upconversion of flicker noise, PMOS transistor is used for the tail current source and a large capacitor is used in shunt with the current source transistor. A 3b capacitor array switch is used for the tuning of the oscillation frequency. The current-mode logic dividers and the resistive output loads are used in the 1.8GHz divide-by-2 circuit. The loop bandwidth of the phase-locked loop is set to 30kHz by adjusting an external resistor and capacitors. The settling time of the synthesizer is less than 40μs.

Figure 11.6.5 shows the measured phase noise of the frequency synthesizer and the output spectrum of the transmitter. The frequency synthesizer achieves the phase noise of –87dBc/Hz at 100kHz offset and –120dBc/Hz at 1MHz offset. The spectrum at the output of the drive amplifier satisfies the required spectrum mask as shown in Fig. 11.6.5. The measured performances of the fabricated transceiver are summarized in Fig. 11.6.6. The RF transceiver consumes 4mA in the receiver chain, 31mA in the transmitter chain, and 26mA in the frequency synthesizer from a 1.8V supply. The receiver front-end P_{1dB} of +8dBm is measured at the normal-mode operation. The measured IIP3 and IIP2 of the receiver front-end are +18.5dBm and +43dBm, respectively. Linearity is significantly improved by using a passive switching mixer. The linearity performance is sufficient for the mobile RFID reader application. Figure 11.6.7 shows the photograph of the single-chip RFID reader IC, fabricated in a 1P6M 0.18μm CMOS process. The die area of the single-chip transceiver is $4.5\times5.3mm^2$ with the RF transceiver area of $2.5\times4.0mm^2$.

Acknowledgements:
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[2] ISO/IEC 18000-6:2004/FPDAM 1 Radio-Frequency Identification for Item Management – Part 6: Parameters for Air Interface Communications at 860 MHz to 960 MHz, 2004.
[3] EPC Class 1 Generation 2 UHF Air Interface Protocol Standard Version 1.0.9, http://www.epcglobalinc.org/standards, 2005.
[4] U. Karthaus and M. Fischer, "Fully Integrated Passive UHF RFID Transponder IC With 16.7-μW Minimum RF Input Power," *IEEE J. Solid-State Circuits*, vol.38, no.10, pp. 1602-1608, Oct., 2003.
[5] S. Zhou and M.-C.F. Chang, "A CMOS Passive Mixer With Low Flicker Noise for Low-Power Direct-Conversion Receiver of IF," *IEEE J. Solid-State Circuits*, vol.40, pp.1084-1093, May, 2005.

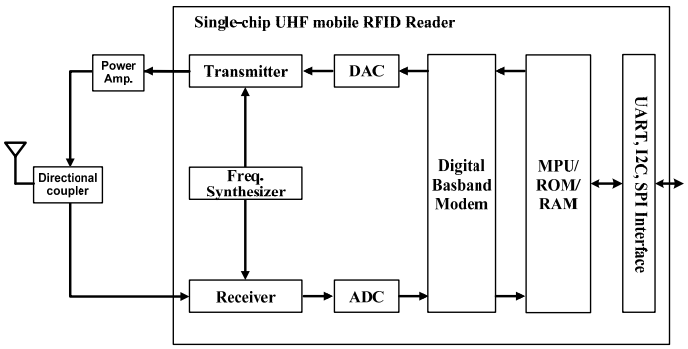

Figure 11.6.1: Block diagram of the single-chip mobile RFID reader.

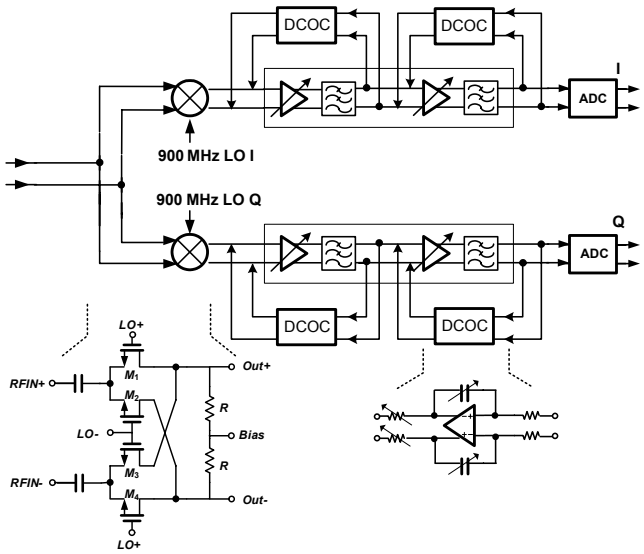

Figure 11.6.2: Receiver architecture.

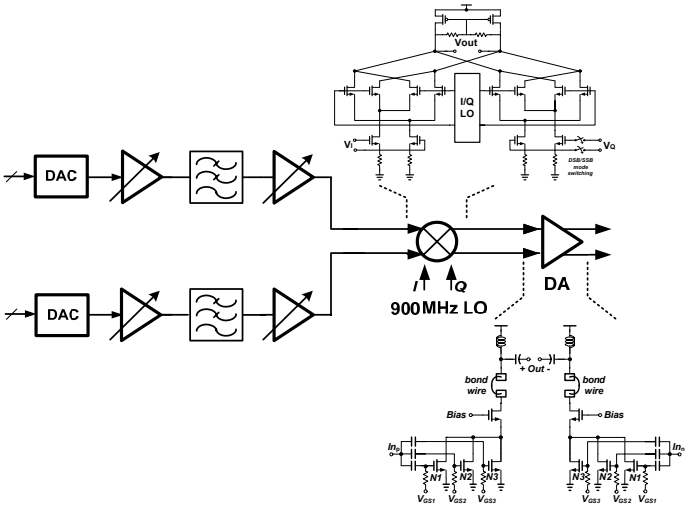

Figure 11.6.3: Transmitter architecture.

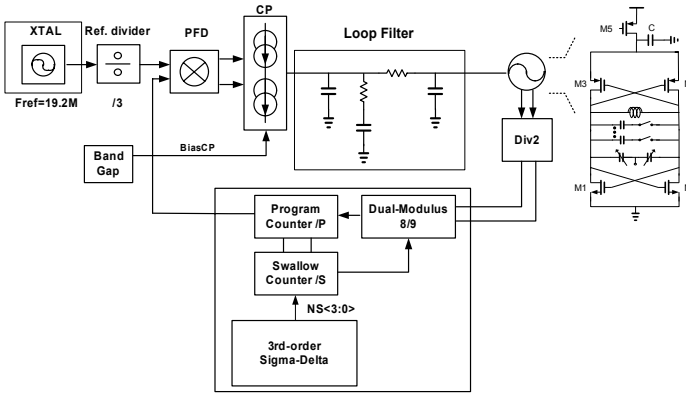

Figure 11.6.4: Frequency synthesizer architecture.

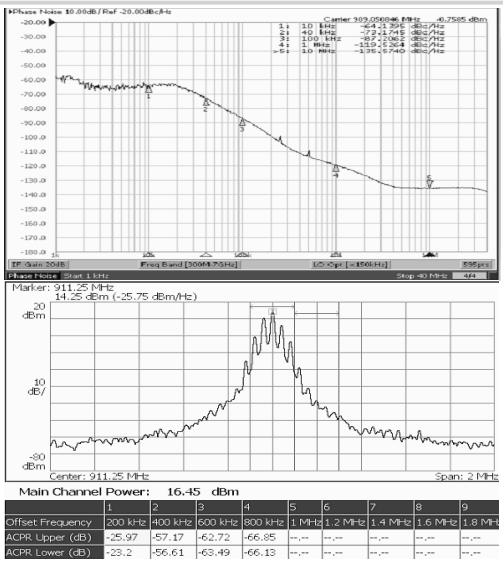

Figure 11.6.5: Measured phase noise and TX output spectrum.

Supply voltage	1.8V
Current consumption (1.8V)	
TX chain	31mA @P_{out}= 4dBm
RX chain	4mA
Synthesizer	26mA
Digital + ADC,DAC	28mA
Total	89mA
RX sensitivity	-70dBm
P1dB (RF front end)	8dBm
IIP3 (RF front end)	18.5dBm
RX gain range	10 ~ 82.5dB
TX output power (DA output)	-9 ~ 4dBm
Synthesizer phase noise	-87dBc/Hz @100KHz offset -120dBc/Hz @1MHz offset
Die size (single-chip IC)	4.5 × 5.3mm^2
Technology	0.18μm 1P-6M CMOS

Figure 11.6.6: Measured performance summary.

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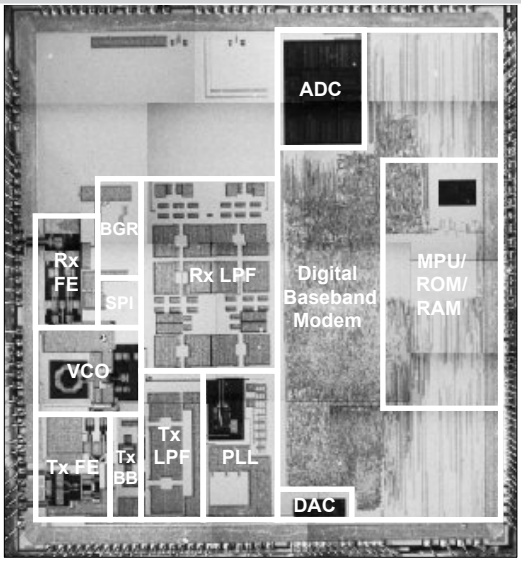

Figure 11.6.7: Chip micrograph.

